Sidereal day = 23h 56'04·090548 (GMT)

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Making a sidereal clock

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A method for constructing a digital sidereal clock is discussed.

Introduction

In a letter to the Editor of this journal[1] Mr C. J. R. Lord comments that, 'it is evident that a degree of Ludditism persists with regard to observatory clocks and setting circles'. There seems little doubt that he is right and it is indeed surprising that so many amateur observers are prepared to spend valuable time in working out sidereal time from tables with the necessary daily and hourly corrections, setting up computer calculations or setting the telescope initially on a star of known right ascension, especially in a country whose climatic vagaries place available observing time at such a premium.

In a previous letter[2] Mr Lord outlined a method of converting a commercial analogue clock driven by a quartz oscillator to run at the sidereal rate, as described by A. A. Mills[3]. However, there is an alternative approach: the construction of a digital clock based on the 50-Hz mains frequency. It is perhaps not generally realised that considerable trouble is now taken by the electricity authorities to maintain the long-term stability of the frequency rate with clocks and other devices in mind. Although a frequency drift within the permitted tolerance of 1% (49.5 to 50.5Hz) may exceptionally occur at times of heavy demand, any temporary frequency deviation is subsequently corrected. The long-term frequency stability is good and better than that of the quartz-driven oscillator, the frequency stability of which can give rise to an error of $\pm$ 5 min/year unless special precautions are taken against temperature and humidity fluctuations and external fields. The long-term accuracy of the mains-driven clock is certainly fully adequate for the setting of telescope R. A. circles.

The required sidereal rate is 366.2422/365.2422 = 1.002737909 of the solar rate. Information in the literature as to how this might be achieved seems rather sparse but Newton[4] showed how this could be done by counting 365 pulses and then slipping in an extra pulse to give a sidereal rate of 1.0027379, an error of 36 per year. Subsequently, Dupuy[5] in the USA devised a 60-Hz mains clock based on a more accurate system, in which four times 365.25 (1461) pulses are counted and four extra pulses are then slipped in to give an error of only 1.8 s per year, as discussed by Reid and Honeycutt[6].

The author decided to construct a sidereal clock from the circuit published by Dupuy but found that, in the rapidly developing field of solid state devices, some of the microchips specified had already become virtually obsolete, necessitating certain minor alterations to the original circuit to allow use of microchips available in this country. Although these changes seemed straightforward enough initially, in fact, a good deal of troublesome debugging had to be carried out with an oscilloscope before satisfactory operation was achieved. It therefore seemed worthwhile to publish details of how this clock may be made, both for those who may not have had access to the original description, and to save those interested unnecessary trouble. The basic design is, however, that of Dupuy and no originality is claimed by me. It is certainly easy for any amateur, who has reasonable ability, to assemble electronic components and construct this clock at a very reasonable cost even if his knowledge of solid state circuitry, like mine, is somewhat superficial!

Clock module

The system is centred on a digital clock module; a suitable device is available in this country (RS No.307-402). This has a 18-mm display (LED), may be programmed to give a 24-h display and set to work at 50 rather than 60 Hz. Four digits only are provided but a toggle switch allows a display of either hours and minutes or minutes and seconds. A battery back-up system for use in the event of power failure can be added but, as this activates an internal oscillator with a wide frequency tolerance ($\pm$ 20%), it is safer to reset the clock, which indicates power interruption by flashing. A specially wound transformer (RS No.207-920) is necessary, which has two secondary windings, one 3.5-

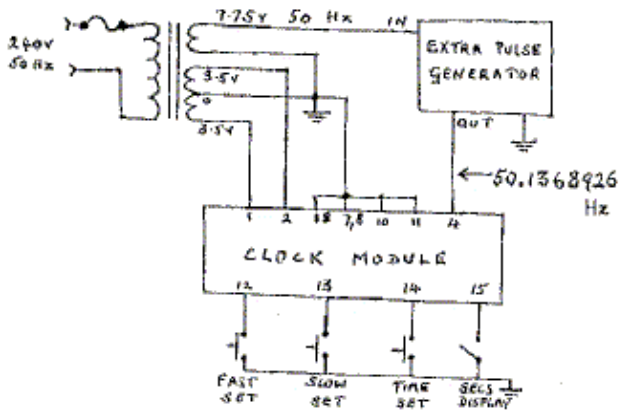

Figure 1. General arrangement of clock module showing intervening extra pulse generator to increase mains frequency to sidereal rate.

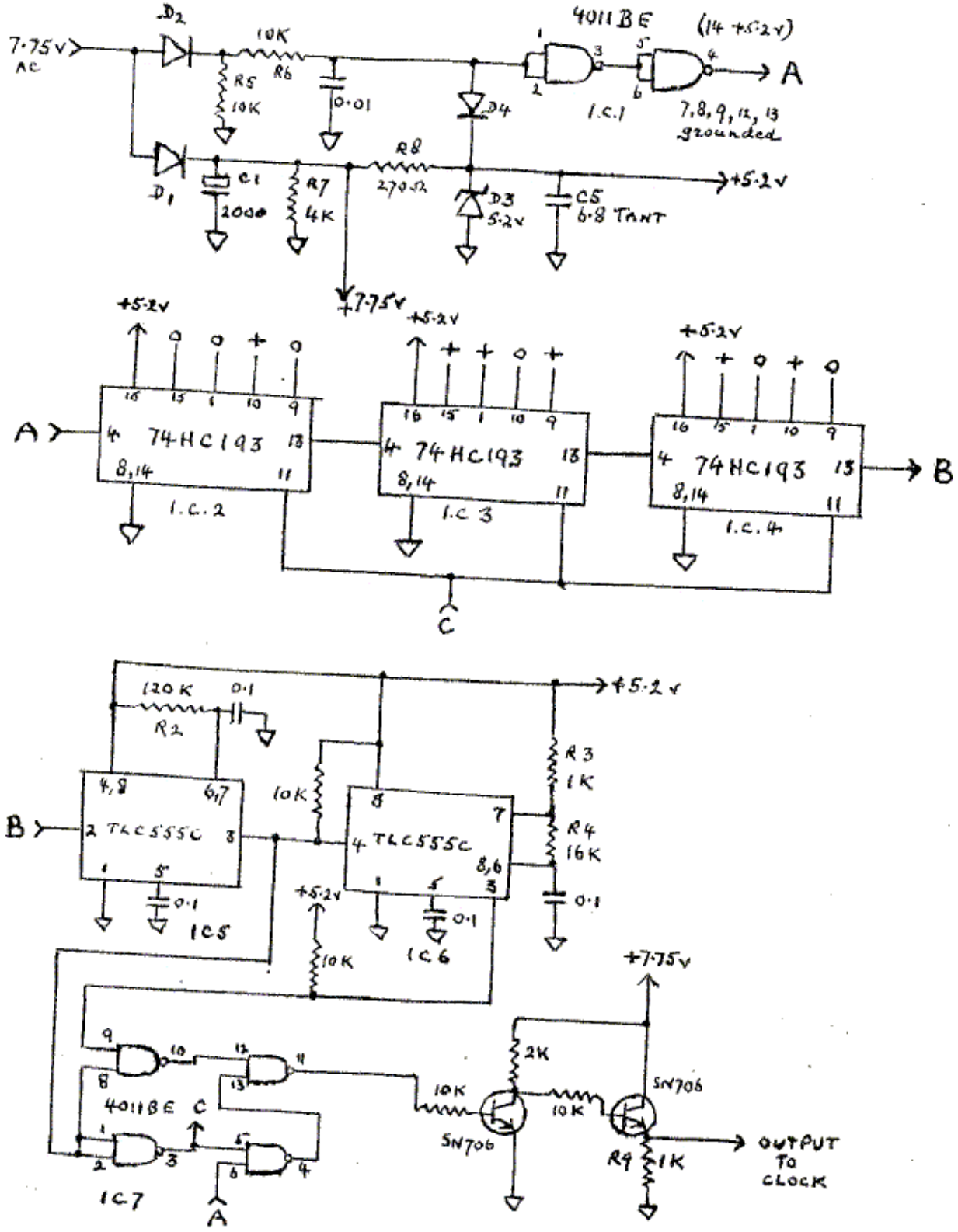

Figure 2. Circuit diagram of the extra pulse generator.

0–3.5 V, which activates the LED display, and the other 0–7.75 V, which powers and triggers the clock module (and in this instance the added counting components). The general arrangement is shown in Figure 1, which depicts the extra pulse-generator to increase the 50-Hz frequency to the sidereal rate. This extra circuitry does not require its own power supply, being powered by the 7.75 V transformer input.

Circuitry and logic

The modified circuit of the extra pulse-generator is shown in Figure 2. The first snag encountered was that the original circuit specified CMOS counter chips, which accept a supply voltage up to 18 V; these have now been largely supplanted by HCMOS chips, with a

maximum supply voltage of only 6 V, necessitating arrangements to reduce the voltage on the input 7.75 V line. On the other hand, the clock module would not perform at less than the full voltage (7.75 V) at the output stage. Normal TTL chips cannot be used, as this would overload the transformer.

The 7.75 V input from the transformer is rectified by D1/C1 and applied to the transistor output stage. This voltage is reduced by Zener diode D3/R8 to 5.2 V for the supply of all microchips. The smoothing capacitator C5 is essential, otherwise the counters will not function.

D2 and its following filter provide a 50-Hz logic signal to IC 1, D4 clipping the pulses to the 5.2 V level. IC 1 acts as a Schmitt trigger and inverter; sections c and d are not used and the inputs must be grounded.

ICs 2, 3 and 4 are three cascaded four-bit binary programmable up-or-down counters and are arranged to count down (from a figure of 1460) via the count-down input at pin 4. The preset initial values are programmed on pins 15(D0), 1(D1), 10(D2), and 9 (D3); note that the preset value, reading from right to left on the diagram, is binary 0101 1011 0100 = Hex 5B4 = 1460. Pins 2, 3, 6 and 7 (outputs) are not used in this application. When the counters have counted down to zero, the next pulse produces a low 'borrow' on pin 13 of IC 4, which triggers the timer IC 5 and is ultimately used to reload the counters with the preset values via line C, with repetition of the count-down cycle.

For extra pulse-generation and timing, Dupuy has developed an ingenious arrangement of the two 555 timers ICs 5 and 6. IC 6 oscillates in unstable mode at 430 Hz but is normally held off by IC 5. IC 5 working as a monostable multivibrator has a gate time of approximately 9 ms so that, when triggered, it allows the development of exactly four pulses from IC 6.

IC 7 inverts the output of IC 6 and issues the load signal to the counters via line C. It also operates as an OR gate, passing either the 50 Hz or the extra pulses to the output transistors that drive the clock.

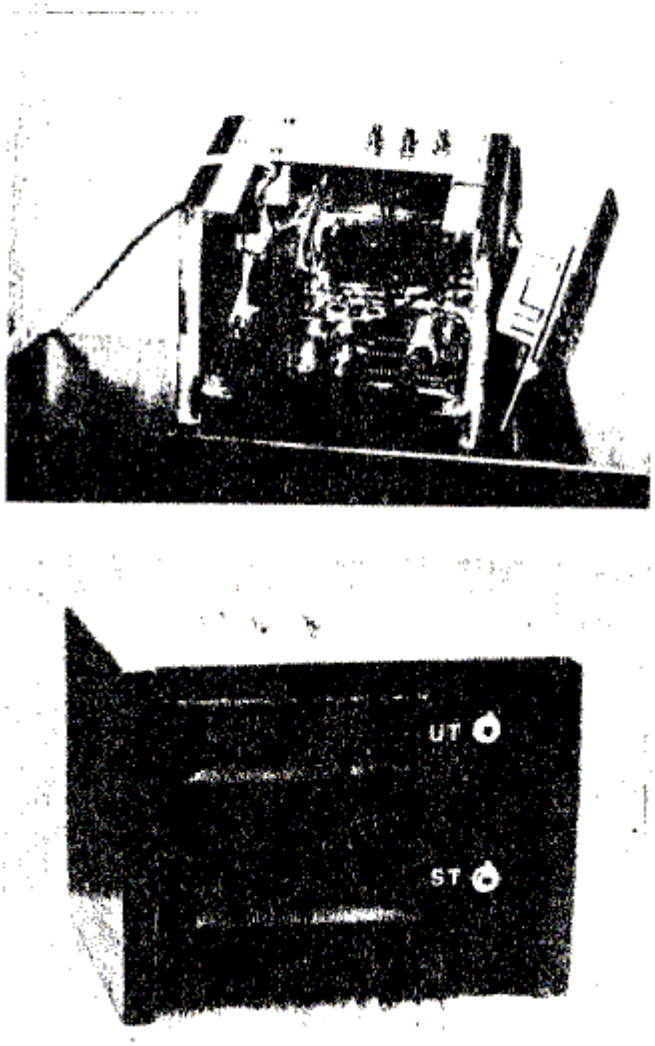

Figure 3. Completed clock with dual display.

Construction

The circuit is sufficiently simple to allow drawing by hand in etch-resist on a single-sided PCB. It is best to use 1% metallized film resistors throughout, although only R4 (controlling oscillator frequency) and R2 (gate time) are at all critical. It was found necessary to increase R2 from the original value of 82 kΩ to obtain satisfactory operation for the 555 timer used (the formula being: gate time = $0.69RC$ where R is in ohms and C in farads). R9 also had to be changed from the original design to get reliable triggering of the clock module with the transistor used. The capacitors associated with the timers should be polystyrene. The usual antistatic precautions should be taken when handling the CMOS chips, which should be mounted in sockets. Press-button switches serve for time-set functions; a miniature SP/ST toggle switch is best for seconds display.

One additional note of warning: do not mount the PCB very close to the mains transformer. This was done on a prototype, where, to save space, the board was mounted in a lid forming the back of the box and almost touching the transformer. This unexpectedly led to scrambling of the counters from the transformer field, the clock failing to function every time the lid was put on!

It is convenient to provide two clock modules, one to read UT (or GMAT), as shown in Figure 3, but a single sidereal readout does of course considerably reduce the cost.

Finally, tribute should be paid to David Dupuy, whose electronic expertise has placed such a valuable and reliable device on our hands.

References

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